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EXAMINER	
PHILPOTT, JUSTIN M	

ART UNIT	PAPER NUMBER
2665	11

DATE MAILED: 08/06/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/553,966	WARD, KENNETH A.	
	Examiner	Art Unit	
	Justin M Philpott	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 June 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-11* is/are allowed.

6)☒ Claim(s) *12-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed June 3, 2004 have been fully considered but they are not persuasive.

First, applicant argues (page 14, fifth paragraph continued to page 15) that duplicating queues Q0-Q7 in Christensen would not create intermediate levels of the hierarchical channel map as recited in claims 12 and 29-31, and one or more intermediate levels recited in claims 12, 29 and 30 are not duplicate parts of Christensen providing a multiplied effect of either top level or lowest level of the hierarchical channel map. However, in the previous office action, Examiner rejected applicant's claims on the basis that the top level and lowest level stages of Christensen provide for an organized system, and accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to include additional organizational stages within the hierarchy of Christensen in order to provide additional organization for a multiplied effect. That is, Examiner contends that at the time of the invention it would have been obvious to one of ordinary skill in the art to utilize the organization of the stages of Christensen to provide an additional organizational stage yielding additional organization for a multiplied effect, and not to provide additional queues Q0-Q7 in the same lowest level or a copy of one of the same levels as applicant has contested. Thus, applicant's argument is not persuasive.

Second, applicant argues (page 15, first paragraph) that Christensen does not teach organized stages. However, Christensen clearly teaches such an organizational stage, wherein register 46 has eight bit positions 0-7 which correspond to the eight queues Q0-Q7 in MS23 (see

col. 6, lines 26-28). Further Christensen contemplates additional elements by disclosing "the concepts taught herein can easily be extended to a multiprocessor with more than two CPs and more than one SC, wherein the CI controller in each SC resolves contentions among all CPs for each queue" (col. 16, lines 24-27). Clearly, an embodiment having a plurality of SCs (i.e., each comprising a register 46) would encourage an additional organizational stage wherein an additional register would comprise bit positions corresponding to one of the plurality of SCs, as provided by Christensen via the existing organization of the register 46 with respect to the queues Q0-Q7. Thus, applicant's argument that Christensen does not teach organized stages is not persuasive.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 18-23 and 25-28 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,271,468 to Christensen et al.

Regarding claim 18, Christensen teaches a system for servicing a communication queues comprising: a memory (e.g., channel interrupt queues Q0-Q7 within main storage 23) configured to store a hierarchical channel map comprising a plurality of levels, wherein one bit of the lowest level is mapped only to a different one of a plurality of communication channels (e.g., each entry in a queue corresponds only to one of a channel interrupt which corresponds to

one of a plurality of communication channels), and wherein each bit of each higher level (e.g., bits PND(0) – PND (7)) is mapped to a group of bits at the next lower level (e.g., each PND bit maps to a particular one of queues Q0-Q7) (e.g., see col. 5, line 53 – col. 8, line 27); a host adapter (e.g., channel controller 24 in FIG. 1) configured to maintain the hierarchical channel map, wherein each bit at the lowest level is set if the channel to which it is mapped has a pending communication request and is cleared if not (e.g., see col. 6, lines 3-17), and wherein each bit of each higher level is set if at least one bit is set in the lower level group to which it is mapped and is cleared if not (e.g., see col. 6, line 24-50); and wherein the host adapter is configured to examine the hierarchical channel map to determine a next one of the communication channels to service (e.g., channel controller 24 generates SIGI command which identifies the queue on which an entry will be posted for a received interrupt, wherein entries are serviced according to the order in which they are placed on the queue, see col. 5, line 65 – col. 6, line 17).

Regarding claim 19, Christensen further teaches the host adapter (e.g., CC 24) is configured to service for one service unit a channel request (e.g., I/O interrupt request) from a channel mapped to a set bit at the lowest level (e.g., an entry among one of the groups of Q0-Q7) of the hierarchical channel map, wherein the set bit is selected by examining a current group of bits at the lowest level of the hierarchical channel map to select a next set bit in that group indicating a channel with a pending request (e.g., a next entry within the designated queue among Q0-Q7), and if no more bits are set in the current group (e.g., the designated queue is empty), examining a current group at the next higher level (e.g., examine next bit of the PND register 46) to select a next set bit (e.g., next bit among PND(0)-PND(7)) and then examining the

next lower level group (e.g., next queue among Q0-Q7 corresponding to the selected PND bit) indicated by the selected higher level set bit (e.g., see col. 5, line 53 – col. 8, line 27).

Regarding claim 20, Christensen teaches a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service mask is configured to indicate the next bit position in the current group to be examined for a set bit (e.g., within the designated queue having the highest non-empty priority).

Regarding claim 21, Christensen teaches each service mask (e.g., via I/O mask 51) is configured to indicate the bit position within the group for the corresponding level of the last selected set bit in that group (e.g., mask 51 indicates the bit position of PND, see col. 6, lines 51-68), wherein the host adapter (e.g., CC 24) is configured to examine each group for the next set bit after the bit position indicated by the corresponding service mask (e.g., see col. 6, lines 24-50).

Regarding claim 22, Christensen teaches each group of bits at one level of the hierarchical channel map has the same number of bits (e.g., each entry in top level, PND register 46, comprises one bit).

Regarding claim 23, Christensen teaches each group of bits at the lowest level (e.g., groups Q0-Q7) is accessible by a single memory access (e.g., see col. 9, line 24 – col. 10, line 21).

Regarding claim 25, Christensen teaches the system as discussed above regarding claim 18 and further teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes (e.g., mask bits configure

communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59), wherein each service class (e.g., designated priority of the queue) is allocated a portion of the limited bandwidth on the communication fabric.

Regarding claim 26, Christensen teaches a service array (e.g., QID register 82) comprising a plurality of entries, wherein each entry indicates one of the service classes to be serviced during a current service unit (e.g., see col. 17, lines 22-30), wherein the service classes are selected in a repeating order according to the entries in the service array, and wherein the next channel to be serviced is selected from the current service class (e.g., see col. 9, line 24 – col. 10, line 31).

Regarding claim 27, Christensen teaches for each service class a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein when its corresponding service class is being serviced each service mask indicates the next bit position to be examined within a selected group of bits to determine a selected group of bits to be examined at the next level (e.g., within the designated queue having the highest non-empty priority), except wherein the service mask for the lowest level indicates the next bit position to be examined within a selected group to determine the next channel with a pending request to be services (e.g., mask bits indicating the next enabled PND bit to be examined).

Regarding claim 28, Christensen teaches a service unit is a quantum smaller than a maximum message size for the channel requests (e.g., I/O interrupt request) (e.g., see col. 5, line 63 – col. 6, line 50, wherein a message size of the interrupt request, SIGI, exceeds the size of a interrupt request entry in the queues Q0-Q7).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 12-17, 24 and 29-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Christensen.

Regarding claims 12-14 and 29, Christensen teaches a system as described above regarding claim 18, however, may not specifically disclose one or more intermediate stages between the highest level and lowest level stages. However, it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect. St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977). The stages of Christensen provide for an organized system, and accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to include additional organizational stages within the hierarchy of Christensen in order to provide additional organization for a multiplied effect. That is, at the time of the invention it would have been obvious to one of ordinary skill in the art to include one or more intermediate stages in the hierarchical channel map of Christensen since it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect.

Further, regarding claim 29, Christensen teaches the system as discussed above regarding claim 18 and further teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a

number of the communication channels to one of a plurality of service classes (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59), wherein each service class (e.g., designated priority of the queue) is allocated a portion of the limited bandwidth on the communication fabric.

Regarding claim 15, Christensen teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes for determining next servicing (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59). Further, Christensen teaches a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service mask is configured to indicate the next bit position in the current group to be examined for a set bit (e.g., within the designated queue having the highest non-empty priority).

Regarding claim 16, Christensen teaches the system as discussed above regarding claim 18 and further teaches a plurality of service class masks (e.g., I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein each service class mask is configured to map a number of the communication channels to one of a plurality of service classes (e.g., mask bits configure communication channels to one of a plurality of queues wherein each queue has a designated priority, see col. 6, lines 51-59), wherein each service class (e.g., designated priority of the queue) is allocated a portion of the limited bandwidth on the communication fabric. Christensen further teaches a service array (e.g., QID register 82) comprising a plurality of entries, wherein each entry indicates one of the service classes to be serviced during a current service unit (e.g.,

see col. 17, lines 22-30), wherein the service classes are selected in a repeating order according to the entries in the service array, and wherein the next channel to be serviced is selected from the current service class (e.g., see col. 9, line 24 – col. 10, line 31).

Regarding claim 17, Christensen teaches for each service class a service mask for each level of the hierarchical channel map (e.g., via I/O mask 51 comprising mask bits, see col. 6, lines 56-67), wherein when its corresponding service class is being serviced each service mask indicates the next bit position to be examined within a selected group of bits to determine a selected group of bits to be examined at the next level (e.g., within the designated queue having the highest non-empty priority), except wherein the service mask for the lowest level indicates the next bit position to be examined within a selected group to determine the next channel with a pending request to be services (e.g., mask bits indicating the next enabled PND bit to be examined).

Regarding claims 24 and 38, Christensen teaches the system of claim 18 as discussed above and, further, teaches the second memory (e.g., PND register 46) is a register comprised within an integrated circuit (e.g., within 22). While Christensen may not specifically require that the integrated circuit comprising the second memory is specifically located within the host adapter (e.g., 24), it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to shift the location of an integrated circuit comprising the second memory from its current position to a position within the host adapter (e.g., 24), since it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. The contention of obvious choice

in design can be overcome if Applicant establishes unexpected results. In re Japikse, 86 USPQ 70 (CCPA 1950).

Regarding claims 30-36, Christensen teaches a system as discussed above regarding claim 18, however, may not specifically disclose channels are further organized into channel sections or one or more intermediate stages are placed between the highest level and lowest level stages. However, it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect. St. Regis Paper Co. v. Bemis Co., Inc., 193 USPQ 8, 11 (7th Cir. 1977). The stages of Christensen provide for an organized system, and accordingly, at the time of the invention it would have been obvious to one of ordinary skill in the art to include additional organizational stages, e.g., organized channels into sections or one or more intermediate stages, within the hierarchy of Christensen in order to provide additional organization for a multiplied effect. That is, at the time of the invention it would have been obvious to one of ordinary skill in the art to include an additional organizational layer in the form of channel sections in the hierarchical channel map of Christensen since it is generally considered to be within the ordinary skill in the art to duplicate parts for a multiplied effect.

Regarding claim 37, Christensen teaches the system of claim 18 as discussed above and, further, teaches the first memory (e.g., Q0-Q7) and the second memory (e.g., PND(0)-PND(7)) are accessible by the host adapter (e.g., CC 24 accesses memory comprised within SC 22 and MS 23). While Christensen may not specifically require both first and second memory to be located on a same memory block, it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to shift the location of the

second memory (e.g., PND) from its current memory position to a memory block comprising the first memory (e.g., Q) since it is generally considered to be within the ordinary skill in the art to shift the location of parts absent a showing of unexpected results. The contention of obvious choice in design can be overcome if Applicant establishes unexpected results. In re Japikse, 86 USPQ 70 (CCPA 1950).

Allowable Subject Matter

6. Claims 1-11 are allowed.

7. The following is a statement of reasons for the indication of allowable subject matter: Claim 1 is allowable for reasons discussed in applicant's remarks (January 9, 2004, pages 15-16) and in the previous office action (March 22, 2004, page 3). Claims 2-11 depend upon, and include further limitations of, claim 1 and are therefore also allowable.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Justin M Philpott

ALPUS H. HSU
PRIMARY EXAMINER